REMARKS

The Office Action dated January 7, 2004 has been received and carefully noted. The above amendments to the claims and the following remarks, are submitted as a full and complete response thereto.

Claims 1-6 are currently amended and pending in the present application. No new matter is presented and no new issues are raised which require further consideration and/or search. Therefore, claims 1-6 are respectfully submitted for consideration.

Claims 1-6 are rejected under 35 U.S.C. 102(a) as being anticipated by the admitted prior art in pages 1-3 and Fig. 1-4 of the specification. The rejection is traversed as being based on reference that neither teaches nor suggests the novel combination of features clearly recited in amended independent claims 1 and 5. Independent claim 1 recites a method for controlling a phase locked loop during change of synchronization source, wherein a fixed setting value of the phase difference is originally set for the phase locked loop. The method comprises the step of changing a synchronization signal from a first synchronization to a second synchronization signal. The method also includes the steps of measuring a phase difference between the second synchronization signal and a signal formed in a phase lock's oscillator and comparing the measured phase difference to a predetermined limit value. The method further includes the steps when the comparing step shows that the measured phase difference is greater than the predetermined limit value, of changing the phase difference between the second synchronization signal and the signal formed from the phase lock's oscillator; repeating

the measuring and comparing steps until the measured phase difference is less than or equal to said predetermined limit value; and when the comparing step shows that the measured phase difference is less than or equal to the predetermined limit value, setting the measured phase difference as a new setting value for the phase difference for use in the normal adjustment function of the phase locked loop instead of the fixed setting value.

Independent claim 5 recites a digital phase lock arrangement, comprising selection components configured to select a desired synchronization source from a set of at least two different synchronization sources. The arrangement also includes a phase comparator having a first and a second input, configured to generate an output signal dependent on a phase difference between signals supplied to the inputs. The arrangement further includes controllers configured to form a control word in response to an output signal which is dependent on the phase difference; and an oscillator, which is controlled with the aid of the control word, the controllers comprising setting components configured to set a measured phase difference as a new setting value for a normal adjustment function of the phase lock arrangement instead of a fixed setting value of the phase difference originally set for the arrangement.

The prior art in the specification shows a typical phase lock structure in Fig. 1. Page 1, paragraph 5. The phase lock structure includes a phase difference meter that compares the phase difference between a reference signal P1 and a signal P2 formed by dividing from an oscillator signal P3 and calculates how many pulses of the oscillator

signal P3 can be accommodated between the rising or falling edges of the signals to be compared. Page 1, paragraph 5. The structure also includes a microcomputer that forms a control word for a D/A converter. Page 2, paragraph 1. The D/A converter converts the control word from digital form into analog form and supplies the converted control word to a crystal oscillator which generates the oscillator signal P3. Page 2, paragraph 2. The structure also includes a divider 18 which receives signal P3 from a cut-off circuit of the oscillator signal. Page 2, paragraph 3. If there is a reason to change synchronization source, the microcomputer with signal CUTC prevents the oscillator signal from having access to the divider forming signal P2 at time T. Page 2, paragraph 3. By performing a suitable number of signal cut-off operations and reading the value of the phase difference meter after each cut-off, it is possible to set the phase difference of signals P1 and P2 with an accuracy of time constant T at the average SETM of the phase meter. Page 2, paragraph 3.

Fig. 2 of the admitted prior art illustrates a situation where a cut-off operation taking place during a change of synchronization signal has allocated the phase of signal P2 at a desired value with a precision of time constant T. Page 2, paragraph 5. Fig. 3 illustrates a time slot of the calculation to be performed in the phase difference meter. Page 3, paragraph 1. Fig. 4 illustrates a flow chart of a method for changing the synchronization source in a phase lock. Page 3, paragraph 3.

Applicant respectfully submit that there is at least one significant difference between the admitted prior art and the claimed invention. Claim 1 in part recites the step

of measuring a phase difference between the second synchronization signal and a signal formed in a phase lock's oscillator; comparing the measured phase difference to a predetermined limit value; when the comparing step shows that the measured phase difference is greater than the predetermined limit value, changing the phase difference between the second synchronization signal and the signal formed from the phase lock's oscillator; repeating the measuring and comparing steps until the measured phase difference is less than or equal to said predetermined limit value; and when the comparing step shows that the measured phase difference is less than or equal to the predetermined limit value, setting the measured phase difference as a new setting value for the phase difference for use in the normal adjustment function of the phase locked loop instead of the fixed setting value. Claim 5 in part recites controllers comprising setting components configured to set a measured phase difference as a new setting value for a normal adjustment function of the phase lock arrangement instead of a fixed setting value of the phase difference originally set for the arrangement. Applicant respectfully submit that in the admitted prior art, the setting value is a fixed setting value which is typically programmed at the factory into the phase lock's microcomputer. This is different from the claimed invention where the measured phase difference is set as a new setting value of the phase difference for use in the normal adjustment function of the phase locked loop instead of the fixed setting value.

The Office Action refers to the situation where the phase lock continues to maintain the phase difference at its original setting value SETM. The Office Action

interprets this situation to render known the feature of setting the measured phase difference as a new setting value for the phase difference for use in the normal adjustment function of the phase locked loop instead of the fixed setting value as recited in claims 1 and 5. The specific situation cited in the Office Action relates to a case when no change of synchronization signal is needed. In such a situation, the system in the admitted prior art retains the phase difference value of that moment. Applicant respectfully submits that in the present invention, the measured phase difference is set to replace the fixed setting value. In an embodiment, this measured phase difference might be exactly the same as the fixed setting value. However, this is not checked. According to the claimed invention, the step of replacing the fixed setting value with the measured phase difference always performed and Applicant submits that this is not the same as doing nothing when a change of synchronization signal is not required. Therefore, Applicant respectfully traverses the rejection under 35 U.S.C. §102(a) and asserts that the rejection should be withdrawn because the admitted prior art does not teach each feature of amended independent claims 1 and 5 and hence, dependent claims 2-4, and 6, respectively.

As noted previously, claims 1-6 recite subject matter which is neither disclosed nor suggested in the admitted prior art cited in the Office Action. It is therefore respectfully requested that claims 1-6 be allowed and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by

telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,

Arlene P. Neal

Registration No. 43,828

Customer No. 32294
SQUIRE, SANDERS & DEMPSEY LLP
14TH Floor
8000 Towers Crescent Drive
Tysons Corner, Virginia 22182-2700

Telephone: 703-720-7800

Fax: 703-720-7802

APN:lls

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